IN THE SPECIFICATION

Please make the following corrections to the specification:

The paragraph beginning on Page 10, line 22 is amended as follows:

Figure 3B is an energy band diagram illustrating direct band to band tunneling with low voltages across the gate oxides or gate insulators in conjunction with metal gate or metal capacitor storage nodes having large work functions according to another embodiment of the present invention. Figure 3B illustrates a metal gate or metal capacitor storage node/plate 309 separated by an insulator, e.g. an oxide 301, from a channel region/substrate 307 or second capacitor storage node/plate. According to the teachings of the present invention, the metal gate or metal capacitor storage node/plate 309 includes a metal gate selected from the group consisting of cobalt, nickel, rubinium-ruthenium, rhodium, palladium, iridium, platinum and gold. Alternatively, in one embodiment of the present invention, the metal gate or metal capacitor storage node/plate 309 includes a metallic nitride gate selected from the group consisting of titanium nitride, tantalum nitride, tungsten nitride, and molybdenum nitride.

The paragraph beginning on Page 12, line 16 is amended as follows:

Figure 5, is a graph plotting work function versus atomic number for large work function materials. Figure 5 is provided to note the relationship of work functions to atomic number and position in the periodic table. Figure 5 illustrates plots the work function versus atomic number of p-type silicon, aluminum (Al), p-type germanium, cobalt (Co), nickel (Ni), rubinium ruthenium (Ru), rhodium (Rh), palladium (Pd), iridium (Ir), platinum (Pt) and gold (Au).

The paragraph beginning on Page 13, line 24 is amended as follows:

Figure 6 can similarly illustrates another embodiment for DRAM device 600, or transistor 601 according to the teachings of the present invention. As shown in Figure 6 a transistor 601 is provided having a first source/drain region 608 and a second source/drain region 610. According to the embodiment shown in Figure 6, the first 608 and the second 610 source/drain region

Serial Number: Unknown Filing Date: Herewith

Title: TECHNIQUE TO CONTROL TUNNELING CURRENTS IN DRAM CAPACITORS, CELLS, AND DEVICES

include source/drain regions, 608 and 610, formed of a material having a large work function. A channel 607 is located between the first and the second source/drain regions, 608 and 610. A gate 609 opposes the channel 607. According to the teachings of the present invention, the gate 609 includes a gate 609 formed of a material having a large work function. In this alternative embodiment, the gate includes a metal gate selected from the group consisting of cobalt, nickel, rubinium ruthenium, rhodium, palladium, iridium, platinum and gold. Further, the metal gate can include a metallic nitride gate selected from the group consisting of titanium nitride, tantalum nitride, tungsten nitride, and molybdenum nitride.

The paragraph beginning on Page 14, line 25 is amended as follows:

In an alternative embodiment, at least one of the first and the second plates, 612 and 614 respectively include metal plates. In this embodiment, the metal plates include metal plates selected from the group consisting of cobalt, nickel, rubinium ruthenium, rhodium, palladium, iridium, platinum and gold. In still another embodiment of the present invention, the first and the second plates, 612 and 614 include metallic nitride plates. In this embodiment, the metallic nitride plates, 612 and 614 include metallic nitride plates selected from the group consisting of titanium nitride, tantalum nitride, tungsten nitride, and molybdenum nitride.

The paragraph beginning on Page 15, line 24 is amended as follows:

Alternatively, the first and the second plates 712 and 714 include metal plates selected from the group consisting of cobalt, nickel, rubinium ruthenium, rhodium, palladium, iridium, platinum and gold. Alternatively still, the first and the second plates 712 and 714 include metallic nitride plates selected from the group consisting of titanium nitride, tantalum nitride, tungsten nitride, and molybdenum nitride.

The paragraph beginning on Page 16, line 1 is amended as follows:

Also, as described above, embodiments of the present invention include a gate 709 that includes a metal gate 709 selected from the group consisting of cobalt, nickel, rubinium ruthenium, rhodium, palladium, iridium, platinum and gold. Alternatively, the gate 709 includes a metallic nitride gate 709 selected from the group consisting of titanium nitride, tantalum

Qi.

Serial Number: Unknown Filing Date: Herewith

Title: TECHNIQUE TO CONTROL TUNNELING CURRENTS IN DRAM CAPACITORS, CELLS, AND DEVICES

nitride, tungsten nitride, and molybdenum nitride. Alternatively still, the gate 709 includes a p-type polycrystalline semiconductor gate selected from the group consisting of p-doped silicon, p-doped germanium, p-doped silicon germanium compounds, p-doped silicon carbide, p-doped silicon oxycarbide compounds, p-doped gallium nitride compounds, and p-doped gallium aluminum nitride compounds.

The paragraph beginning on Page 19, line 12 is amended as follows:

Alternatively, in one embodiment, forming the first and the second storage nodes includes forming the first and the second storage nodes of a metal selected from the group consisting of cobalt, nickel, rubinium ruthenium, rhodium, palladium, iridium, platinum and gold.

The paragraph beginning on Page 19, line 20 is amended as follows:

In one embodiment, forming the gate includes forming a metal gate selected from the group consisting of cobalt, nickel, rubinium ruthenium, rhodium, palladium, iridium, platinum and gold. In another embodiment of the above method forming the gate includes forming a metallic nitride gate selected from the group consisting of titanium nitride, tantalum nitride, tungsten nitride, and molybdenum nitride. In another embodiment of the above method forming the gate includes forming a p-type polycrystalline semiconductor gate selected from the group consisting of p-doped silicon, p-doped germanium, p-doped silicon germanium compounds, p-doped silicon carbide, p-doped silicon oxycarbide compounds, p-doped gallium nitride compounds, and p-doped gallium aluminum nitride compounds.

In all locations listed above, please delete the word "rubinium" and substitute the word "ruthenium." Applicant respectfully submits that this substitution is typographical in nature and does not constitute new matter. Applicant notes that the chemical symbol for ruthenium (Ru) is used in a number of locations in the specification, and that the atomic number of ruthenium (44) is indicated in Figure 5.

PRELIMINARY AMENDMENT

Serial Number: Unknown Filing Date: Herewith

Title: TECHNIQUE TO CONTROL TUNNELING CURRENTS IN DRAM CAPACITORS, CELLS, AND DEVICES

Respectfully Submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. Box 2938

Minneapolis, MN 55402

(612) 373-6944

Date //-25-03

D :110 D :

David C. Peterson Reg. No. 47,857

"Express Mail" mailing label number: EV298565322US

Date of Deposit: November 25, 2003

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to The Commissioner for Patents, Mail Stop Patent Application, P.O. Box 1450, Alexandria, VA 22313-1450.